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10/523,257	01/27/2005	Elstan Anthony Fernandez	2002 P 05725 US	8306

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EXAMINER	
TRAN, THANH Y	
ART UNIT	PAPER NUMBER
2822	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/05/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/523,257	ELSTAN ANTHONY FERNANDEZ	
	Examiner	Art Unit	
	Thanh Y. Tran	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *26 September 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6,9-12 and 14-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-2, 5-6, 9-12, and 14-20* is/are rejected.

7)☒ Claim(s) *3 and 4* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-2, and 7-9 are rejected under 35 U.S.C. 102(e) as being anticipated by Kawamura et al (U.S. 6,566,760).

As to claim 1, Kawamura et al discloses in figures 5 a semiconductor package including a substrate ("module substrate"), an integrated circuit (uppermost "memory chip") mounted on the substrate ("module substrate"), a heat conductive plate ("lead") having a portion (see the lower portion of "lead" underneath the two memory chips) interposed between the integrated circuit (uppermost "memory chip") and the substrate ("module substrate"), the heat conductive plate ("lead") being heat-conductively connected to the integrated circuit (uppermost "memory chip") and having at least one portion (see the end portion of "lead" which is attached to surface of "module substrate") extending laterally out from between the integrated circuit (uppermost "memory chip") and the substrate ("module substrate"); and a second integrated circuit (lower "memory chip") disposed between the plate ("lead") and the substrate ("module substrate"), the plate ("lead") being in heat-conductive contact with the second integrated circuit (lower "memory chip"), whereby heat generated by the second integrated circuit (lower

"memory chip") is conducted away from the second integrated circuit (lower "memory chip") by the plate ("lead").

As to claim 2, Kawamura et al discloses in figures 5 a semiconductor package in which the integrated circuit (uppermost "memory chip") is encased in resin ("sealing resin"), the plate ("lead") extending out of the resin ("sealing resin"), whereby heat generated in the integrated circuit (uppermost "memory chip") is conducted out of the resin ("sealing resin").

As to claim 7, Kawamura et al discloses in figures 5 a semiconductor package, further comprising: a second integrated circuit (lower "memory chip") disposed between the plate ("lead") and the substrate ("module substrate").

As to claim 8, Kawamura et al discloses in figures 5 a semiconductor package, in which the plate ("lead") is in heat-conductive contact to the second integrated circuit (lower "memory chip"), whereby heat generated by the second integrated circuit (lower "memory chip") is conducted away from the second integrated circuit (lower "memory chip") by the plate ("lead").

As to claim 9, Kawamura et al discloses in figures 5 a semiconductor package in which the second integrated circuit (lower "memory chip") is a flipchip.

3. Claim 10 is rejected under 35 U.S.C. 102(e) as being anticipated by Huang et al (U.S. 2002/0074672).

As to claim 10, Huang et al discloses in figures 5G-5H a semiconductor package and a corresponding method of forming a plurality of semiconductor packages, comprising: securing a heat-conductive plate ("die pad layer" 14) over a substrate (11),

mounting a plurality of integrated circuits (1) over the heat-conductive plate ("die pad layer" 14) with a heat-conductive connection therebetween, the heat conductive plate ("die pad layer" 14) having at least one portion extending laterally out from between the integrated circuits (1) and the substrate (11), the plate (14) extending between each of the integrated circuits (1) and the substrate (11); and cutting the substrate (11) and the plate (14) to produce a plurality of semiconductor packages (figure 5H) each including at least one of the integrated circuits (1).

4. Claims 14, and 18-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Shibata (U.S. 2001/0035569).

As to claim 14, Shibata discloses in figures 1(a)-3 a packaged semiconductor device comprising: a substrate (as indicated at 7 in figure 5) including a plurality of contact regions (8) on an upper surface; a heat conductive plate (comprising "die pad portion" 1a, and 1g) mounted over the substrate (as indicated at 7 in figure 5), the heat conductive plate (1a, 1g) comprising a central portion (1a) and a plurality of arms (1g, figure 1(b)) extending outwardly from the central portion (1a), one or more of the arms (1g) extending laterally outwardly from a side surface of the central portion (1a) of the plate; an integrated circuit (3) having a bottom surface mounted over the central portion (1a) of the heat conductive plate; and a plurality of electrical connections (4) between an upper surface of the integrated circuit (3) and the contact regions (as shown in figure 5) of the substrate, the electrical connections (4) extending between adjacent ones of the arms (1g) of the heat conductive plate.

As to claim 18, Shibata discloses in figures 1(a)-3 a packaged semiconductor device, wherein the electrical connections (4) comprise wire bonds.

As to claim 20, Shibata discloses in figures 1(a)-3 a packaged semiconductor device, wherein the central portion (1a) of the heat conductive plate is affixed to the integrated circuit (3) by heat-conductive glue (5) and wherein the central portion (1a) of the heat conductive plate is affixed to the substrate (as indicated at 7 in figure 5) by heat-conductive glue (device 10 is "directly soldered through solder reflow" to the printed circuit board, see paragraph [0003]).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kawamura et al (U.S. 6,566,760) in view of Ohsawa et al (U.S. 2002/0031862).

As to claim 6, Kawamura et al does not disclose the plate includes at least one portion of increased thickness laterally outward from the integrated circuit.

Ohsawa et al discloses in figures 2A-2D a semiconductor package comprising a plate (comprising elements 2 and 3) includes at least one portion (3) of increased thickness laterally outward from the integrated circuit ("LSI chip" 7). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the semiconductor package of Kawamura et al by having a plate that includes at least one portion of increased thickness laterally outward from the

integrated circuit as taught by Ohsawa et al for supporting the semiconductor package when the semiconductor package is mounted a motherboard.

7. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kawamura et al (U.S. 6,566,760) in view of Joshi (U.S. 4,069,498).

As to claim 5, Kawamura et al does not disclose the plate is grounded and electrically connected to at least one ground input of the integrated circuit.

Joshi discloses in column 1, lines 36-39 a heat plate is grounded ("ground potential") and electrically connected to at least one ground input of the integrated circuit ("chip"). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the semiconductor package of Kawamura et al by having a heat plate is grounded and electrically connected to at least one ground input of the integrated circuit as taught by Joshi for providing a good heat mechanism or good electrical conductors, and enhancing the heat transfer from the chip (col. 1, lines 45-68 in Joshi)

8. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kawamura et al (U.S. 6,566,760) in view of Papageorge et al (U.S. 5,438,224).

As to claim 19, Kawamura et al does not disclose a plurality of balls disposed on a lower surface of the substrate, each of the balls electrically coupled to a respective one of the contact regions.

Papageorge et al discloses in figure 1 a packaged semiconductor device comprising: a plurality of balls ("bumps" 159 disposed on a lower surface of the substrate

(150), each of the balls (159) electrically coupled to a respective one of the contact regions (152). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Kawamura et al by having a plurality of balls disposed on a lower surface of the substrate, each of the balls electrically coupled to a respective one of the contact regions as taught by Papageorge et al for coupling the IC assembly or semiconductor package to circuitry of the external circuit board (see col. 5, lines 40-53 in Papageorge et al).

9. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Huang et al (U.S. 2002/0074672) in view of Kawamura et al (U.S. 6,566,760).

As to claim 11, Huang et al does not disclose a semiconductor package, in which after mounting the integrated circuit to the heat-conductive plate, the integrated circuit is embedded in resin, the heat-conductive plate extending laterally out of the resin.

Kawamura et al discloses in figure 5 a semiconductor package, in which after mounting the integrated circuit ("memory chip") to the heat-conductive plate ("lead"), the integrated circuit (("memory chip") is embedded in resin ("sealing resin"), the heat-conductive plate ("lead") extending laterally out of the resin ("sealing resin"). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the device of Huang et al by having a heat-conductive plate extending laterally out of the resin after mounting the integrated circuit to the heat-conductive plate, and the integrated circuit is embedded in resin for providing an easy mount/connection between the packages and the printed circuit board.

10. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Huang et al (U.S. 2002/0074672) in view of Sano et al (U.S. 5,952,714).

As to claim 12, Huang et al does not disclose a semiconductor package in which prior to securing the heat-conductive plate to the substrate a second integrated circuit is mounted on the substrate, the heat-conductive plate being secured to the substrate with the second integrated circuit between a portion of the plate and the substrate.

Sano et al discloses in figure 5 a semiconductor package and a corresponding method in which prior to securing the heat-conductive plate ("lead frame" 24) to the substrate (42) a second integrated circuit ("chip" 41) is mounted on the substrate (42), the heat-conductive plate (24) being secured to the substrate (42) with the second integrated circuit (41) between a portion of the plate (24) and the substrate (24). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the semiconductor package of Huang et al by having the step of: prior to securing the heat-conductive plate to the substrate a second integrated circuit is mounted on the substrate, the heat-conductive plate being secured to the substrate with the second integrated circuit between a portion of the plate and the substrate as taught by Sano et al for providing an easy assembling process for the semiconductor package.

11. Claims 15-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shibata (U.S. 2001/0035569) in view of Araki et al (U.S. 6,828,661).

A to claims 15-17, Shibata does not disclose the packaged semiconductor device, wherein the heat conductive plate further comprises a rim portion that surrounds the central portion and is thermally connected to the central portion by the plurality of arms,

the heat conductive plate includes four diagonal arms, each diagonal arm extending outwardly from a corner of the central portion to the rim portion; and the heat conductive plate further includes four lateral arms, each lateral arm extending outwardly from a side surface of the central portion of the plate to the rim portion.

Araki et al discloses in figure 2a a packaged semiconductor device, wherein the heat conductive plate (13) comprises a rim portion (13a) that surrounds the central portion (23b) and is thermally connected to the central portion (23b) by the plurality of arms (23c), the heat conductive plate (13) includes four diagonal arms (23c), each diagonal arm (23c) extending outwardly from a corner of the central portion (23b) to the rim portion (13a); and the heat conductive plate (13) further includes four lateral arms (23c), each lateral arm (23c) extending outwardly from a side surface of the central portion (23b) of the plate to the rim portion (13a). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the device of Shibata by including a rim portion that surrounds the central portion as taught by Araki et al for providing a sufficient mechanical strength or reliability of the resin-sealed semiconductor device (see col. 7, lines 32-59 in Araki et al).

Allowable Subject Matter

12. Claims 3-4 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

13. Applicant's arguments with respect to claims 1-6, 9-12, and 14-20 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

14. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh Y. Tran whose telephone number is (571) 272-2110. The examiner can normally be reached on M-F (9-6:30pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on (571) 272-2429. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TYT

Zandra V. Smith
Supervisory Patent Examiner
22 Dec. 2006